Pad and FEE side update

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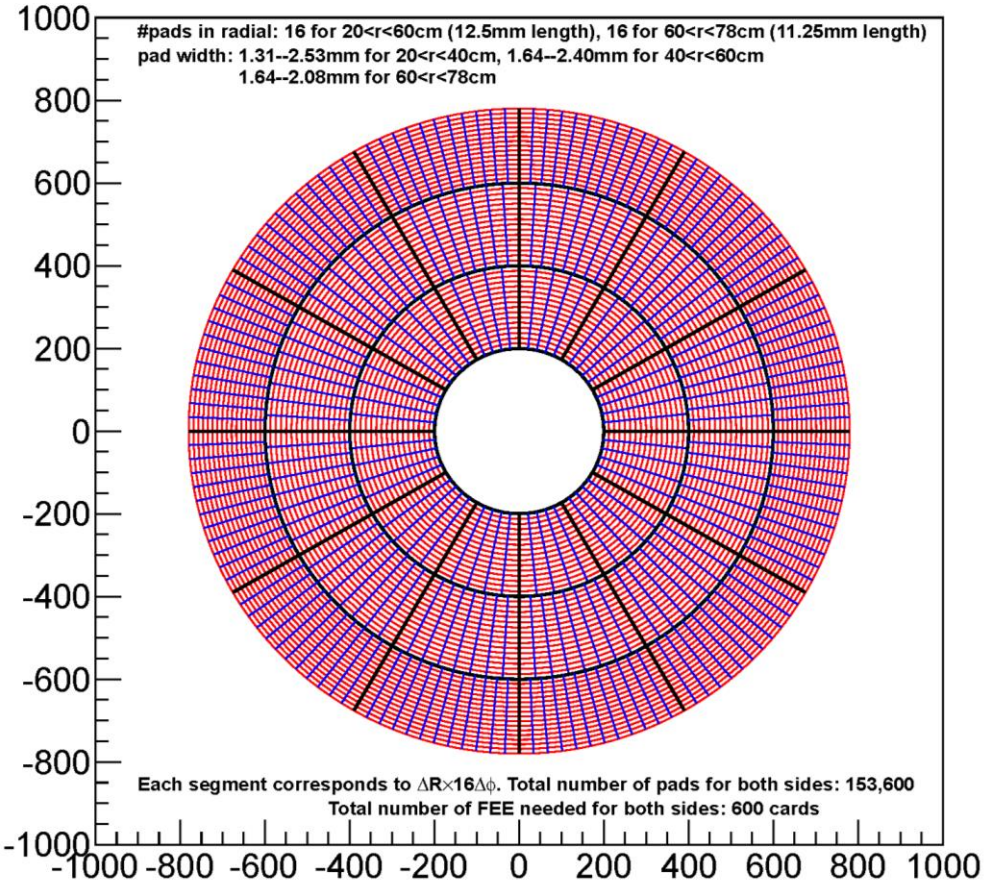
Pad side update

- New pad layout (20<r<78cm)
  - Three segments in radial direction, each divided into 16
  - 12 segments in phi direction, each divided into multiple of 16
  - Matching to number of input to a FEE
  - Each cell in the right figure corresponds to 16 pads in phi
- Variable pad size as a function of radial position
- Total 153,600 pads for both side
  - 600 FEE cards
- Data Rate (no header included)
  - 1.42Gbps/board for 30<r<40cm
  - 1.45Gbps/board for 40<r<60cm
  - 0.77Gbps/board for 60<r<80cm
  - → 28Gbps/(1/12 full azimuth)

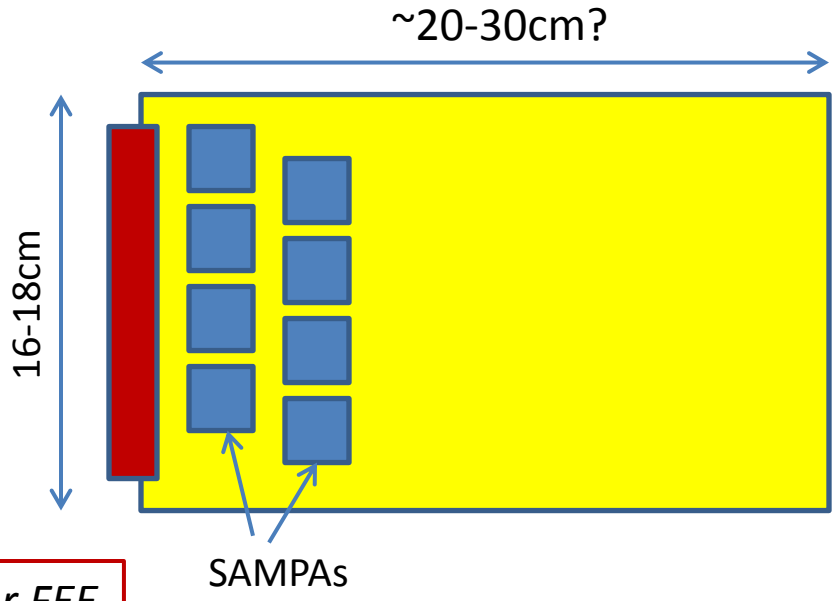
5 FEEs for 20<r<40cm, 8 for 40<r<60cm, 12 for 60<r<78cm, for each 1/12 of full azimuth

Each cell = 16pads in phi



FEE side update

- 256 channels per card (eight SAMPAs) is the fixed number
- From the previous pad layout, the minimum spacing of the FEE cards will be ~2cm (at r=20cm)
  - This is acceptable from the point of view of engineering
- Width of FEE card will be ~16-18cm
  - The most outer radial segment will be 60-78cm
  - Cable from pad to SAMPA should be less than 5 inches (STAR's experience)
- GBT or other protocol?
  - If we put FPGA on the FEE, the optical doesn't need to be GBT
  - FPGA would have SEU. STAR's experience tells one serious SEU event happens every 10 minutes.



We should start engineering for FEE